SOI CMOS-based Transistor Model for Low Power Wireless Sensor Network

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Introduction: The major challenge in wireless networks is the finite energy of the sensor node which is by and large engaged in transmitting and receiving data. It is known that substantial amount of energy is consumed in transmitter portion as shown in Figure - 1. A further analysis revealed that the Low Noise Amplifier, as shown in Figure - 2, a constituent unit of the transmitter, consumes the bulk of the power.

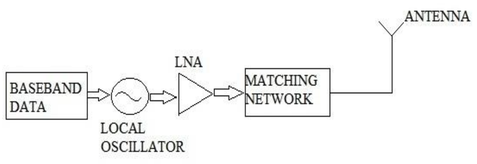

Figure 1. OOK transmitter

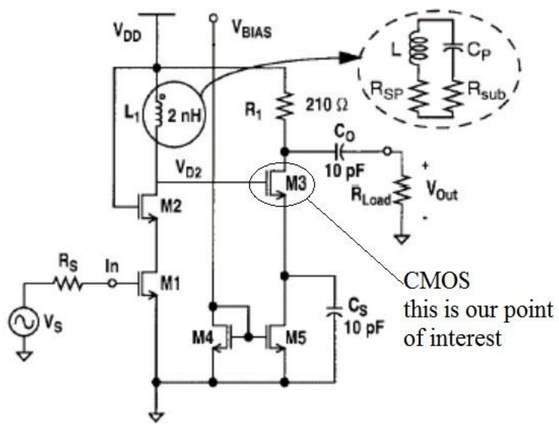

Figure 2. Expanded version of LNA

Research attempts have been made to reduce the drain current, which in turn reduces the power, and internal capacitance with the help of SOI CMOS. The advantage of SOI CMOS is that it has a buried oxide layer above silicon layer which helps in reducing the capacitance as well as drain current.

Proposed Models: In order to minimize the power consumption further, two SOI CMOS based topologies have been proposed in this work.

1.The Hole Model:

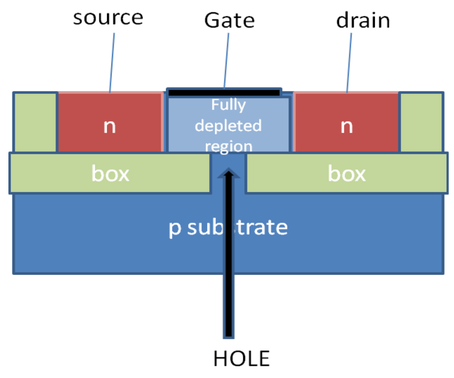

Figure 3. The Hole Model

In this model, the oxide layer has been split into two parts leaving a hole in between layers as shown in the figure above. The hole in the middle provides path for the current in a controlled manner and the oxide layers on both the sides help in reducing the internal capacitance.

2.The Sandwich Model:

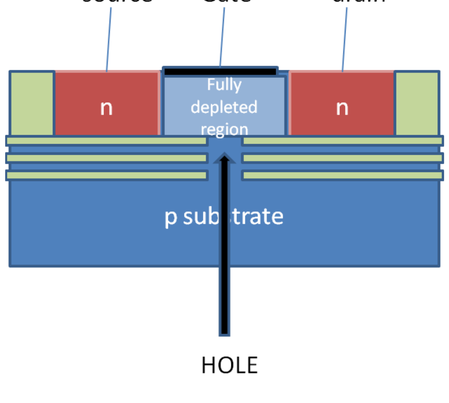

Figure 4. The Sandwich Model

In this model, there are three oxide layers sandwiched above the substrate. Besides there is a hole in between oxide layers. Therefore this model can be viewed as a three oxide layers with holes as shown in Figure - 4. This will help in reducing the capacitance and efficient heat dissipation as well.

Results: The proposed topologies have been simulated in COMSOL Multiphysics Software Version 3.5 by taking bulk Si-CMOS model from COMSOL model library as reference. The drain current with respect to voltage was analyzed for each model.

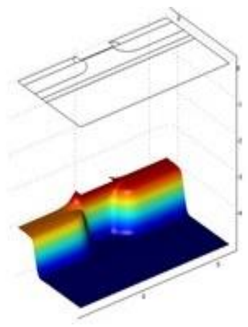

Figure 5. Voltage Distribution in SOI CMOS

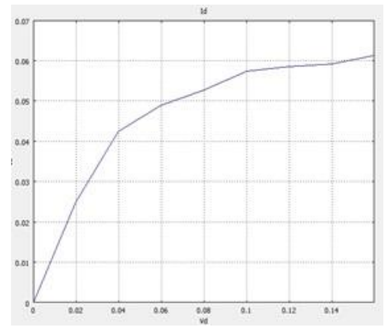

Figure 6. Vd – Id Characteristics of SOI CMOS

Figures – 5 & 6 represent the Voltage Distribution and Vd – Ids characteristics for SOI CMOS. It has been observed that the saturated drain current is 60mA.

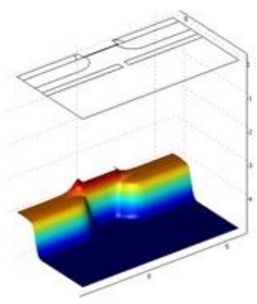

Figure 7. Voltage Distribution in Hole Model

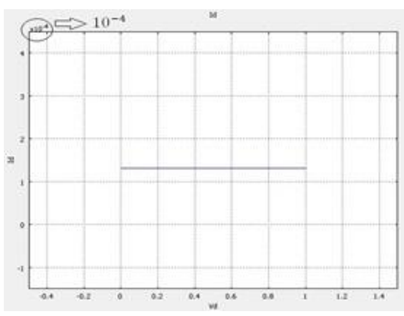

Figure 8. Vd – Id Characteristics of Hole Model

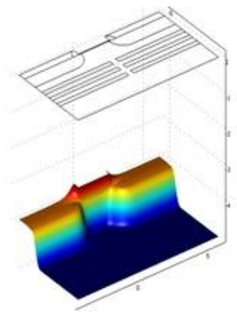

Figure 9. Voltage Distribution in Sandwich Model

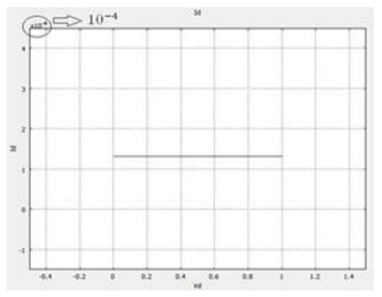

Figure 10. Vd – Id Characteristics of Sandwich Model

Figures – 7, 9 and 8, 10 represent the voltage distribution and Vd – Ids characteristics for the Hole and Sandwich model and it was observed that the saturated drain current is 0.125mA which is very less than that of SOI CMOS.

Conclusion: The two proposed topologies exhibited reduced drain current as compared to the Bulk and SOI CMOS models. It has also been observed that the drain current is a function of the distance of separation between two oxide layers. Thus these topologies will be very much useful in designing LNA for the sensor nodes.

References:

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