Logic Gate Simulation for Fluidic Computers

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Abstract

Computing provides a special-purpose computing paradigm and is integrated on small-scale microfluidic platforms. Because of their very small size, fluidic computers have a number of advantages and potential. Fluidic computers works on fluids such as air, water etc. and does not depend on electrical power traditional semiconductor electronics based computers. The major aim of fluidic computing is to enhance the functionality of different applications, by integrating a computing capability with the inherent advantages of microfluidics. Here, simulations on the operation of basic fluidic logic gates are performed in COMSOL Multiphysics platform and all the possible combinations for the logic operations are tested and are compared with the corresponding truth table. A fluid is pressurized from the inlet of a microfluidic channel and the valves perpendicular to the channel are pressurized to control the flow operations as per the required logic operations. The inlet pressure of the fluid is taken as 1 Pa and the valve pressure to create deflection of its diaphragm is considered as 1.2 Pa. The deflection of the diaphragm of the valve closes the pathway of the fluid flowing and thus provides 'logic 0' where as the flow of fluid is considered as 'logic 1'. These independent logic gates can be assembled for large fluidic computations in a proposed fluidic computer. Though fluid-based computing does not aim to replace traditional silicon-based technology, computing elements, but will serve to the communities in the remote areas proving them the digitized computation capability and thus leading to technological advancement. To date, most of these have been fabricated at the microscale[1-4], but as applications develop, many of these could be further shrunk to significantly smaller, nano-fluidics sizes for more precise and rapid computations.

Reference

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Figures used in the abstract

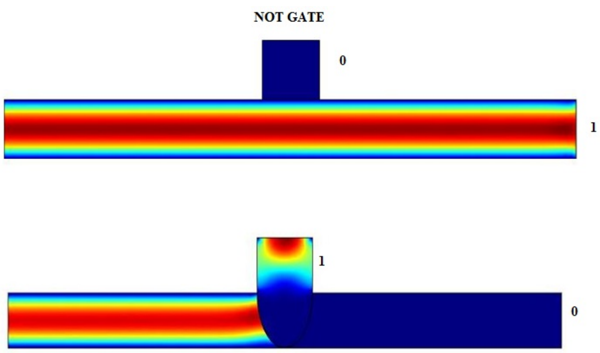

Figure 1: Fluidic NOT gate showing when valve is pressurized no flow at the output and logic gets inverted.

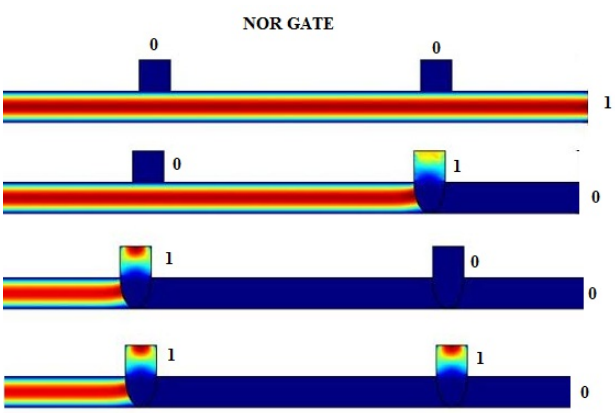

Figure 2: Fluidic NOR gate showing all possible inputs and corresponding outputs.

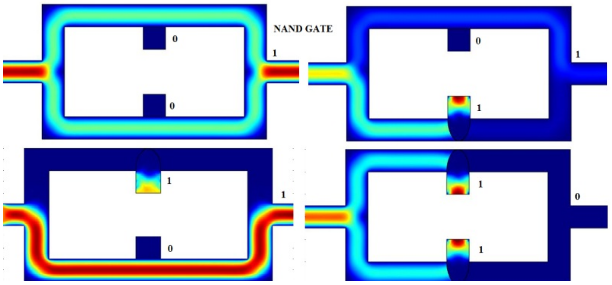

Figure 3: Simulation results for fluidic NAND gate with all input cases.

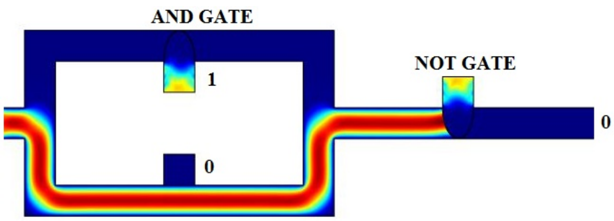

Figure 4: Fluidic AND gate achieved by adding NOT gate to the output of NAND gate.