J-integral evaluation for cracks in Through Silicon Vias

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Abstract

3D integrated devices pose interesting challenges in terms of reliability investigations and the modelling of potential failure modes. In this work, the delamination possibility of a metal layer along an open through silicon via (TSV) bottom edge is investigated by simulating the most critical step of the thermal cycling test. In this step, stress arises due to different thermal expansion coefficients of the materials that form the TSV. By employing the finite element method, the stress at the TSV edge is calculated. Subsequently, the results are utilized to calculate the energy release rate of a preexisting delaminated area along the conductive layer at the TSVs bottom edge. For this purpose, an appropriate formula for the energy release rate for the axis symmetric geometry of the crack inside the TSV is derived. The influence on the flaw of the geometry of the TSV conductive layer is evaluated and the critical geometrical conditions for delamination occurrence are determined.

Keywords: TSV, J-integral, delamination

1. Introduction

Through Silicon Vias (TSV) are one of the key technologies for 3D integration. They are vertical electrical connections that pass through a silicon wafer and establish the signal transmission between the front and the backside of the device. This technology can be used as a replacement of pads with wire bonding and flip-chip bonding. In comparison to the traditional wire bonding method, TSVs allow to increase the number of electrical components of the whole system and reduce the connection path between these components [1], [2].

In the so-called “TSV last” integration scheme, the TSV processing is done after the processing of the CMOS has been finished. The holes for the TSVs are etched from the backside until the first CMOS metal layer on the frontside is reached. The remaining CMOS backend stack (metal and dielectric layers) form a membrane at the TSV bottom.

The TSV sidewalls are insulated by a dielectric material such as silicon dioxide. In order to achieve the electrical connection, a metal is subsequently deposited by physical and chemical vapor deposition. An additional electrochemical deposition can be used to increase the thickness of the metal. The layer underneath the electrochemical deposited copper is called seed layer. The most common used metals for the TSV last technology are tungsten and copper.

The coefficient of thermal expansion (CTE) mismatch between the metal and silicon substrate [3] can result in reliability concerns due to thermo-mechanical stress. Using open TSVs can support to reduce that risk because the materials can freely expand in the radial direction of the TSVs.

Moreover, the effects of the CTE mismatch are already measurable during the TSV fabrication because the deposition of the different materials such as silicon oxide and metals require different temperatures thus enabling the possibility to induce high mechanical stress. This stress could lead to delamination especially in the case of copper whose CTE mismatch (Table 1) with the surrounding layers is significantly higher compared to tungsten.

Experimental observations of thermal cycling tests (TCTs) with a temperature range of -65 to 175 °C on TSVs with copper metallization and varying geometries showed the delamination of the interface between the electrochemical-deposited metal and the seed layer after 500 cycles (Figure 1 and Figure 2). It is assumed that the observed delamination is a result of the cooling phase to the temperature of -65 °C since it causes the copper to contract. The mismatch of the coefficients of thermal expansion of the layers induces stress in the structure and ultimately the delamination.

When the delamination occurs between the TSV metal and the first CMOS metal layer, the electrical performance of the device is damaged. If the delamination involves the entire interface between the

copper and the first CMOS layer of the membrane, an open circuit is formed. Therefore, it is necessary to establish a process window, which can avoid this failure.

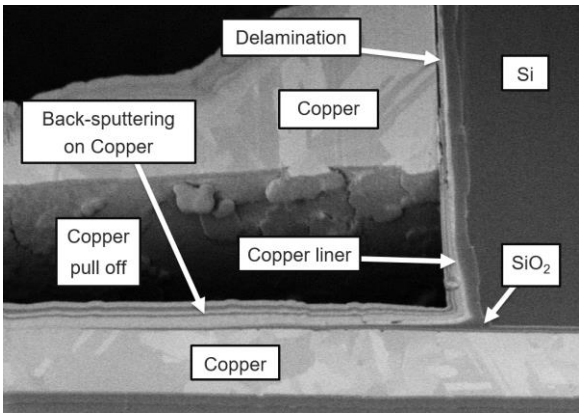

Figure 1: Cross section of a TSV with a diameter of 40 µm after 500 cycles of TCT with a temperature range of -65°C to 175°C. The complete delamination of the copper layer from the copper seed layer can be observed.

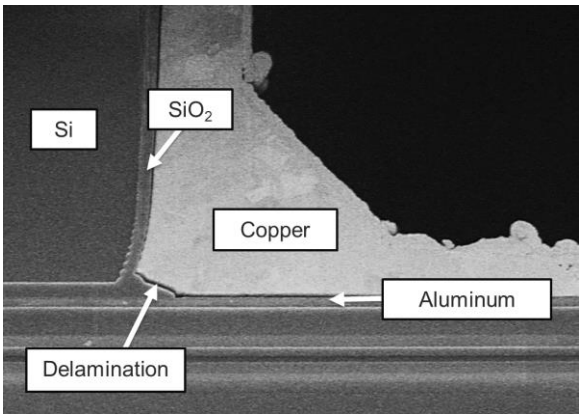

Figure 2: Cross section of a TSV with a diameter of 80 µm after 500 cycles of TCT with a temperature range of -65°C to 175°C. Delamination of the copper layer from the CMOS membrane can be observed.

The effects of the TSV geometry on the delamination probability of copper from the CMOS layer were studied by performing FEM simulations of the TCTs cooling phase in COMSOL Multiphysics.

2. Problem description and finite element model

The simulated geometry of the TSV structure obtained from the standard process is shown in Figure 3. It is an axis symmetric slice of the TSV with a diameter of 40 µm and the neighboring silicon substrate. The TSV axis is oriented along the z-direction and the TSV radius along the radial axis. The mechanical properties of the materials forming the structure are listed in Table 1, which include the CTE, the Young modulus E, the Poisson ratio v and the density. All displacements along the bottom surface of the model are forbidden to avoid the free movement of the body. The lateral side of the model is far enough from the TSV to avoid any influence of its boundary conditions on the stress distribution of the TSV edge.

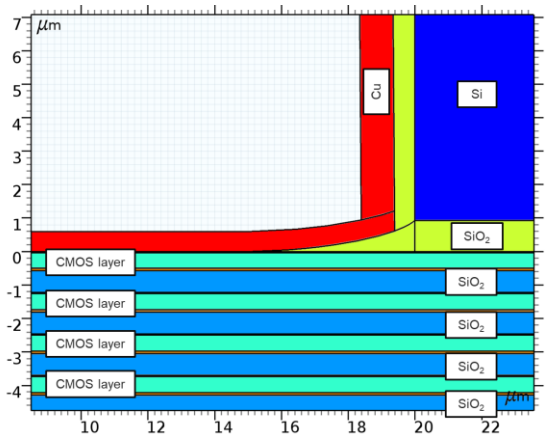

Figure 3: Geometry of the TSV slice, which has been simulated.

Table 1: Material parameters including CTE, the Young modulus E, the Poisson ratio v and the density, which are used in the simulation.

Material	CTE (10^{-6}/K)	E (GPa)	ν	Density (kg/m^3)
Si	2.6	135	0.28	2329
SiO_2	0.5	70	0.17	220
W	4.5	600	0.25	5200
CMOS layer	23	70	0.33	2700
Cu	16.5	120	0.34	8960

From the experimental observations of the TCTs on TSVs with varying geometries, it is deduced that the point where the delamination initiates is close to the TSV corner (Figure 2). Therefore, an initial simulation without a crack is performed to determine the stress distribution at the copper-CMOS interface. This assumption is confirmed by controlling if the stress achieves a peak at the TSV corner.

The thermo-mechanical deformation of the structure for a cooling from 20 to -65 °C was simulated as it is assumed that the structure is stress-free at room temperature. Linear elasticity is used to simulate the mechanical behavior of the structure. The silicon and the silicon oxide are ceramic materials, which obey to this behavior. Non-elastic behavior of the copper layer could change quantitatively the results of the simulation, but it is assumed that the amount of plastic deformation during TCT is small enough to be neglected in the simulation.

In order to evaluate the effects of the geometry of the TCT tested TSV structures on the delamination, the thickness of the copper layer was set to 0.5, 2.5, 5.0, 7.5 and 10 µm and the stress distribution was evaluated.

2.1. Stress distribution

The evaluation of the stress distribution of the copper-CMOS interface after the cooling showed that the axial component of the stress tensor is mainly responsible for the delamination of the interface. Figure 4 shows the axial component of the stress tensor along the radial coordinates of the TSV at the interface for five different copper thicknesses. The axial stress increases moving from the center to the edge of the TSV. This suggests that if delamination occurs, it would most likely initiate close to the TSV corner confirming the experimental observations. Additionally, increasing the copper thickness causes the stress to rise as well.

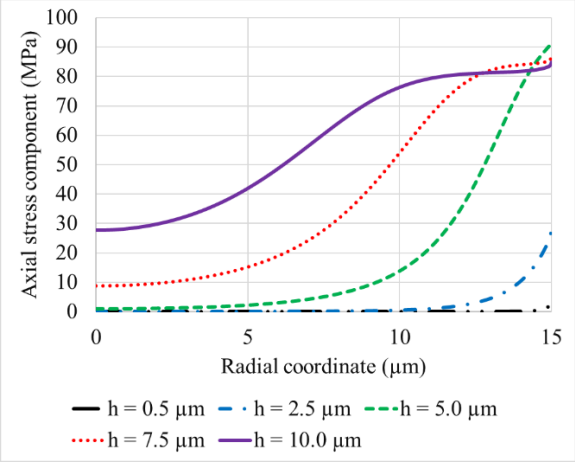

Figure 4: The axial component of the stress tensor along the interface between the copper layer and first CMOS layer for different copper thickness.

Therefore, the model is extended by adding an axial symmetric crack along the interface between the membrane and copper at the TSV edge, which represents the delamination of the copper. The probability of delamination occurrence is determined by the critical value of the energy release rate for different copper thicknesses. The energy release rate can be evaluated through the calculation of the J-integral of the crack tip along the interface between copper and the CMOS layer [4]. It allows to evaluate the influence of all components of the stress tensor on the delamination, quantifying the energy release rate of an already delaminated area.

2.2 J-integral derivation for axis-symmetric structures

In order to derive an appropriate formulation of the J-integral for an axial symmetric crack, which is initiated at a certain radius and runs along the whole angle, the three-dimensional J-integral of Carpenter *et al.* [5] is used as a starting point:

$$J = \oint_S \left[W n_1 - \frac{du_i}{dx_1} \sigma_{ij} n_j \right] ds - \int_A \frac{d}{dx_3} \left(\sigma_{i3} \frac{du_i}{dx_1} \right) dA \quad (1)$$

with the cylindrical coordinates $x_1 = r$ the radius, $x_2 = z$ the height and $x_3 = \phi$ the circumferential angle; n_j the normal vector, u_i the displacements as well as the stress σ_{ij} in r, z and ϕ direction, ds the integral along the contour S, dA the integral along the surface area A due to crack propagation, and W the strain energy release rate (Figure 5).

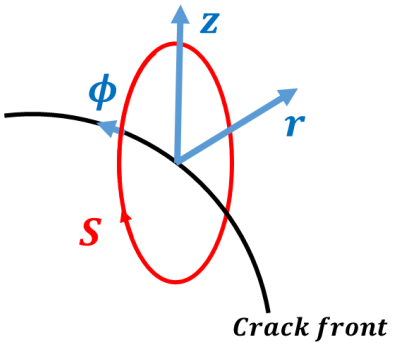

Figure 5: Local cylindrical coordinate system at a point of the crack front.

Since the crack has an axial symmetry, the following simplifications can be made. The displacement u_ϕ and all derivatives along ϕ vanish. It is considered that the contour S lies in a thin slice of the plane $n_\phi = 0$. This means that equation (1) can be transformed to

$$J = \oint_S \left[W n_1 - \frac{du_i}{dx_1} \sigma_{ij} n_j \right] ds \qquad (2)$$

and the second part of the equation becomes

$$\frac{du_i}{dr} \sigma_{ij} n_j = \frac{du_r}{dr} (\sigma_{rr} n_r + \sigma_{rz} n_z) + \frac{du_z}{dr} (\sigma_{zr} n_r + \sigma_{zz} n_z) . \qquad (3)$$

The derived equation (2) is the same as the derived two-dimensional J-integral of Rice [6]. This means that the circumferential stress does not contribute to the delamination probability. In order to verify that this is the case, the J-integral of Carpenter et al. (equation (1)) is implemented in the simulation of an axial symmetric structure and the simplified equation (2) is used in a full 3D model. If the calculated values of the two models for different thicknesses is the same, the simplifications were valid. Furthermore, this would allow to implement the simplified equation of Rice in a non-axial symmetric structure with an axial symmetric crack.

2.3 J-integral calculation

For the axial symmetric and 3D model, the J-integral along three different paths surrounding the crack are evaluated (Figure 6). The integration along the three different paths is used to prove the path-independency property of the J-integral hence the mesh around the three paths is fine enough and the simulation was performed for a cooling sequence from room temperature to -65°C as well as varying copper thicknesses from 0.5 to 10 µm with a step size of 0.5 µm.

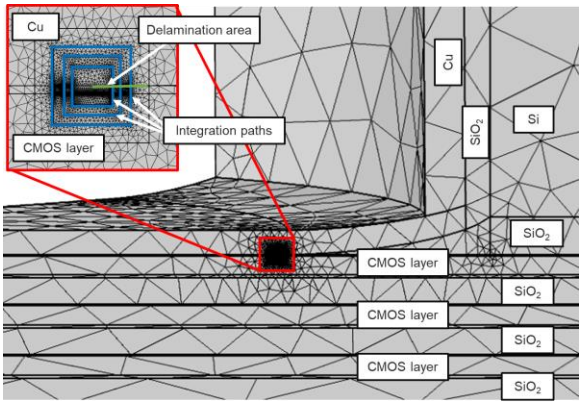

Figure 6: Meshed structure with the layers in evidence. In the inlet, the edge of the pre-existing delaminated area is surrounded by three paths, along which the J-integral is calculated.

Results and discussions

The J-integral values calculated along the three different paths are the same, confirming the path-independency property. Figure 7 shows the J-integrals of an axial symmetric and three-dimensional model for the delaminated area as function of the thickness of the conductive material. The standard deviation of the three J-integral paths for the axial symmetric case has a maximum of 0.9×10^{-4} N/m and for the three-dimensional case 1.3×10^{-4} N/m. The two J-integrals have a maximum offset of 8.1×10^{-4} N/m. Moreover, the integral of the surface area is zero for the applied equation (1) in the two dimensional axial symmetric simulation. This means that the simplification of the J-integral performed in paragraph 2.2 were valid and the equation of Rice can be applied for an axial symmetric crack.

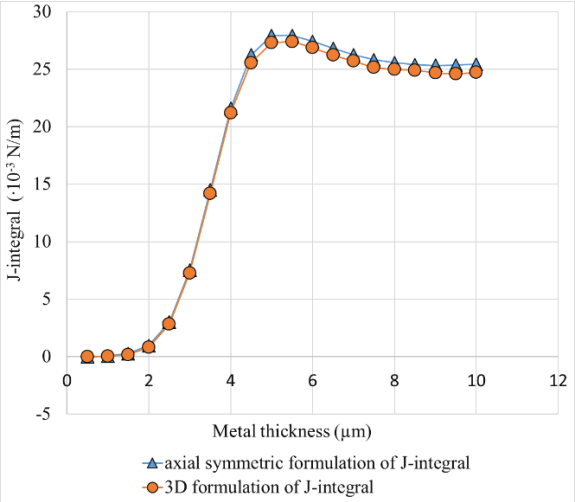

Figure 7: The J-integral calculated along inner path for an axial-symmetric and fully three-dimensional TSV model as function of the copper layer thickness.

Furthermore, the J-integral is nearly constant when the thickness is lower than 2 µm and bigger than 8 µm. The J-integral increases by one order of magnitude when the thickness is higher than 2 µm, significantly raising the likelihood of the delamination during TCTs. When the copper thickness increases beyond 5.5 µm, the J-integral decreases slightly. This coincides with the crack position and its length as it is placed 5 µm far from the TSV corner and has a length of 0.5 µm. This corresponds to the stress distribution in Figure 4, as the z-component of the stress has a maximum at 90 MPa for copper thickness of 5 µm but is reduced to 85 MPa for 7.5 and 10 µm copper thicknesses. This means that if the delamination develops for lower thicknesses during TCTs with conditions that lead to overstressing, an additional increase of the thickness would in reality elongate the lifetime of the delaminated surface.

Implementation of the plastic deformation of the copper could change quantitatively the results but not qualitatively the behavior of J-integral. The reason is that the plasticity lowers the amount of the J-integral but does not shift the position of the stress peak from the TSV edge to other places. This means that the analysis of the influence of copper layer thickness on the crack probability does not change.

Summary and conclusion

Simulations of the stress caused by the cooling cycle of TCTs on open TSVs with varying metal thicknesses showed that the delamination at the TSV bottom most likely occur at the TSV corner.

In order to evaluate the delamination probability for different metal thicknesses, the J-integral for an axial symmetric crack at the TSV edge for a linear elastic material was derived, which resulted in the two dimensional J-integral of Rice. Therefore, the model was extended to the third dimension and the three dimensional J-integral was applied to the axial symmetric model and the simplified model to the three dimensional case. As both simulations resulted in the same value, the derivation was proven to be valid. This allows a simple evaluation of the energy release rate of an axial symmetric crack in a three-dimensional structure.

Furthermore, a suggestion for the process window of the copper thickness for the standard TSV geometry, shown in Figure 3, was established by the evaluation of the J-integral. The metal thickness should be kept below 2 µm because higher values would significantly increase the delamination probability.

References

[1] J. Kraft *et al.*, "3D Sensor application with open through silicon via technology," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 560–566.

[2] C. Cassidy *et al.*, "Through Silicon Via Reliability," *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 2, pp. 285–295, Jun. 2012.

[3] J. V. Olmen *et al.*, "Integration challenges of copper Through Silicon Via (TSV) metallization for 3D-stacked IC integration," *Microelectron. Eng.*, vol. 88, no. 5, pp. 745–748, May 2011.

[4] R. E. Smelser, "On the J-integral for Bi-material bodies," p. 3, 1977.

[5] W. C. Carpenter, D. T. Read, and R. H. Dodds, "Comparison of several path independent integrals including plasticity effects," *Int. J. Fract.*, vol. 31, no. 4, pp. 303–323, Aug. 1986.

[6] J. R. Rice, "A Path Independent Integral and the Approximate Analysis of Strain Concentration by Notches and Cracks," *J. Appl. Mech.*, vol. 35, no. 2, pp. 379–386, Jun. 1968.